

PCA8550

4-bit multiplexed/1-bit latched 5-bit I²C EEPROM DIP switch

Rev. 7 — 8 April 2015

Product data sheet

1. General description

The primary function of the 4-bit 2-to-1 I²C multiplexer is to select either a 4-bit input or data from a non-volatile register and drive this value onto the output pins. One additional non-multiplexed register output is also provided. The non-multiplexed output is latched to prevent output value changes during I²C writes to the non-volatile register. A write protect input is provided to enable/disable the ability to write to the non-volatile register. An “override” input feature forces all outputs to logic 0.

2. Features and benefits

- 4-bit 2-to-1 multiplexer, 1-bit latch DIP switch
- 5-bit internal non-volatile register
- Override input forces all outputs to logic 0
- Internal non-volatile register write/readable via I²C-bus
- Write-protect pin enables/disables I²C writes to register
- 2.5 V multiplexed outputs
- 3.3 V non-multiplexed output (latched)
- 5 V tolerant inputs
- Useful for ‘jumperless’ configuration of PC motherboards
- Designed for use in Pentium Pro/Pentium II systems



3. Ordering information

Table 1. Ordering information

Type number	Topside marking	Package		
		Name	Description	Version
PCA8550D	PCA8550	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
PCA8550DB	PA8550	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
PCA8550PW	PCA8550	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

3.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
PCA8550D	PCA8550D,118	SO16	REEL 13" Q1/T1 *STANDARD MARK SMD	2500	T _{amb} = 0 °C to +70 °C
PCA8550DB	PCA8550DB,118	SSOP16	REEL 13" Q1/T1 *STANDARD MARK SMD	2000	T _{amb} = 0 °C to +70 °C
PCA8550PW	PCA8550PW,118	TSSOP16	REEL 13" Q1/T1 *STANDARD MARK SMD	2500	T _{amb} = 0 °C to +70 °C

4. Block diagram

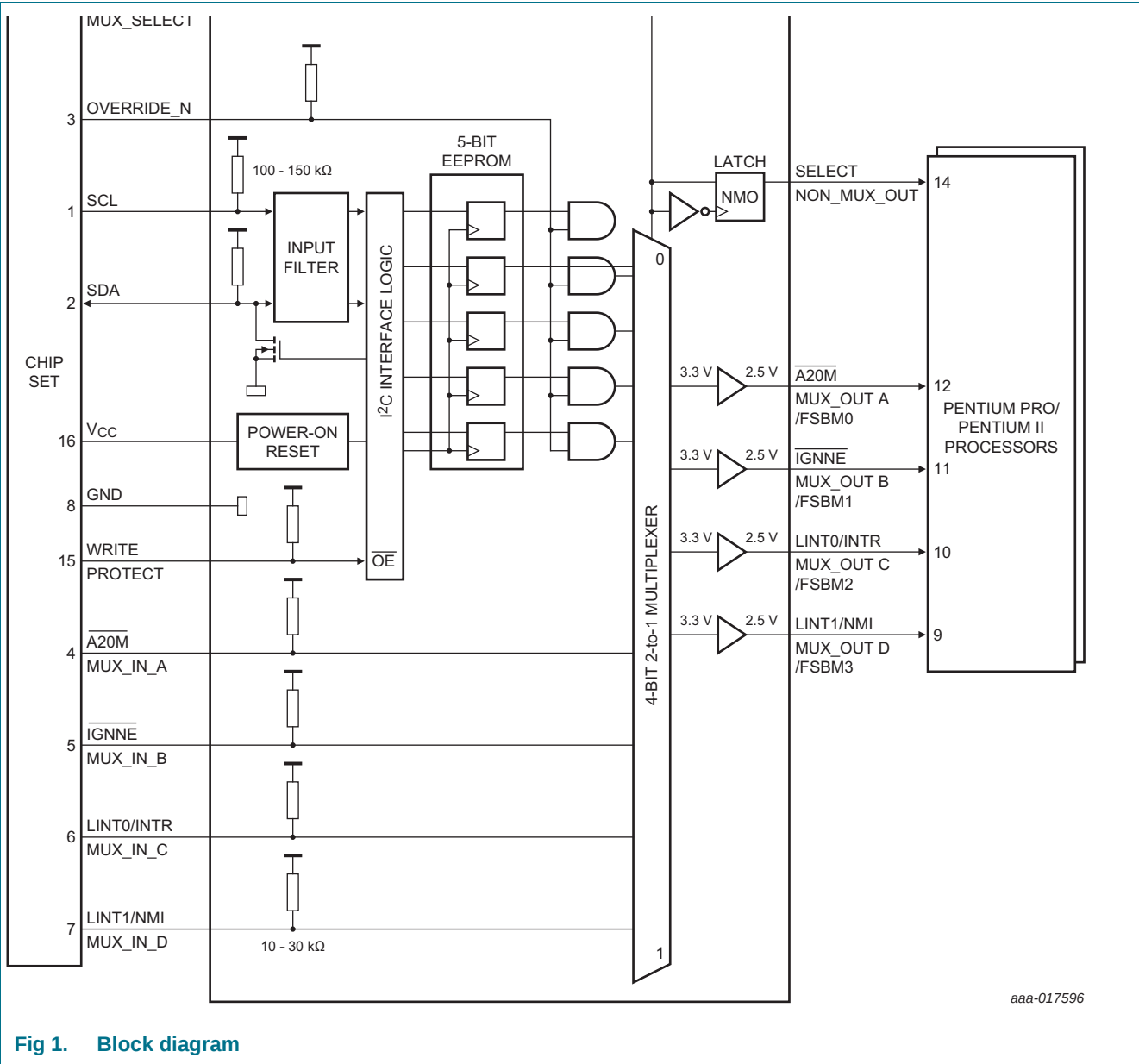


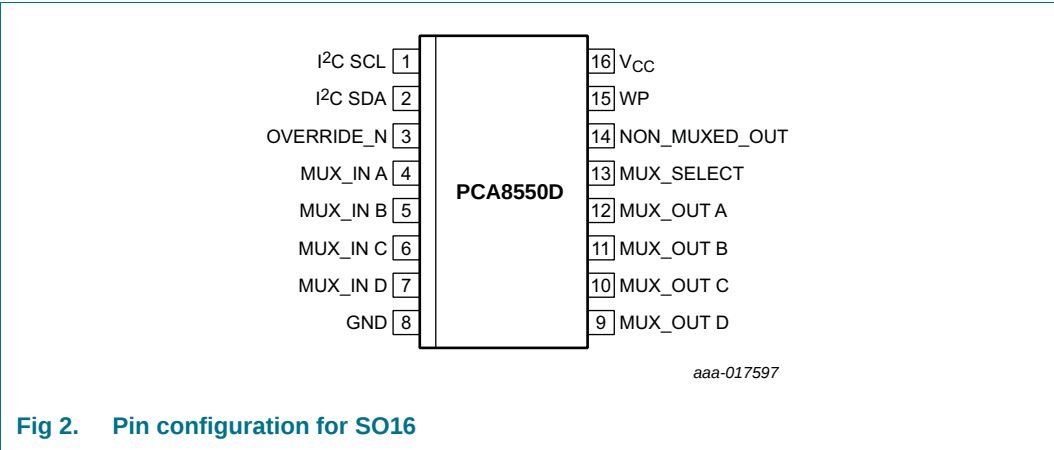
Fig 1. Block diagram

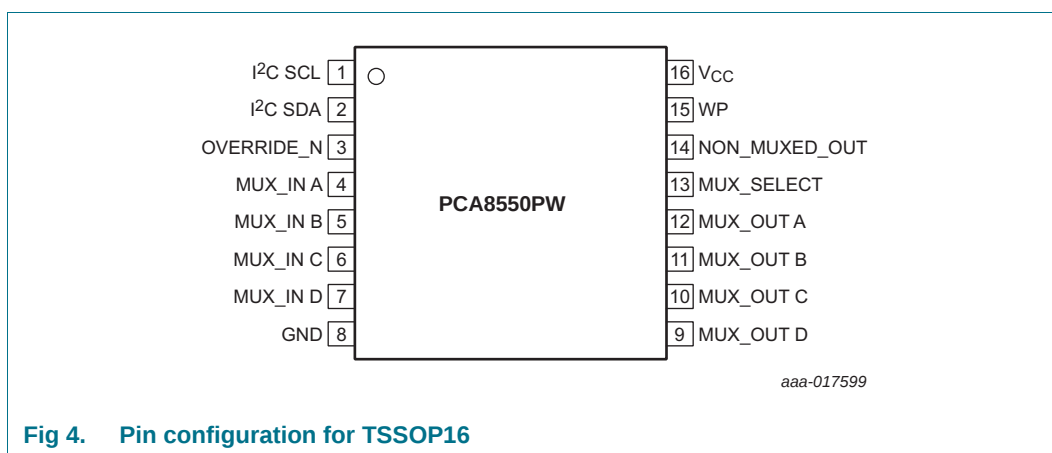
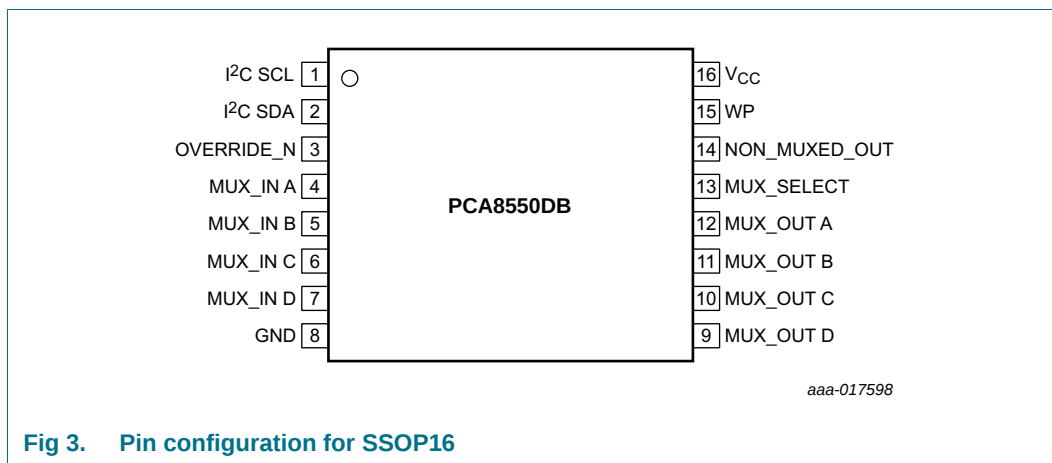
5. Pinning information

5.1 Pin description

Table 3. Pin description

Symbol	Pin	Description
I ² C SCL	1	I ² C-bus clock
I ² C SDA	2	Bi-directional I ² C-bus data
OVERRIDE_N	3	Forces all outputs to logic 0
MUX_IN A	4	External inputs to multiplexer
MUX_IN B	5	
MUX_IN C	6	
MUX_IN D	7	
GND	8	Common ground voltage rail
MUX_OUT D	9	2.5 V multiplexed output
MUX_OUT C	10	
MUX_OUT B	11	
MUX_OUT A	12	
MUX_SELECT	13	Selects MUX_IN inputs or register contents for MUX_OUT outputs
NON_MUXED_OUT	14	TTL-level output from non-volatile memory
WP	15	Non-volatile register write-protect
V _{CC}	16	Positive voltage rail





6. Functional description

When the MUX_SELECT signal is logic 0, the multiplexer will select the data from the non-volatile register to drive on the MUX_OUT pins. When the MUX_SELECT signal is logic 1, the multiplexer will select the MUX_IN lines to drive on the MUX_OUT pins. The MUX_SELECT signal is also used to latch the NON_MUXED_OUT signal which outputs data from the non-volatile register. The NON_MUXED_OUT signal latch is transparent when MUX_SELECT is in a logic 0 state, and will latch data when MUX_SELECT is in a logic 1 state. When the active-LOW OVERRIDE_N signal is set to logic 0 and the MUX_SELECT signal is at a logic 0, all outputs will be driven to logic 0. This information is summarized in Table 1. The write protect (WP) input is used to control the ability to write the contents of the 5-bit non-volatile register. If the WP signal is logic 0, the I²C-bus will be able to write the contents of the non-volatile register. If the WP signal is logic 1, data will not be allowed to be written into the non-volatile register.

The factory default for the contents of the non-volatile register are all logic 0. These stored values can be read or written using the I²C-bus (described in the next section).

The OVERRIDE_N, WP, MUX_IN, and MUX_SELECT signals have internal pull-up resistors. See [Section 9](#) and [Section 10](#) for hysteresis and signal spike suppression figures.

6.1 Function table

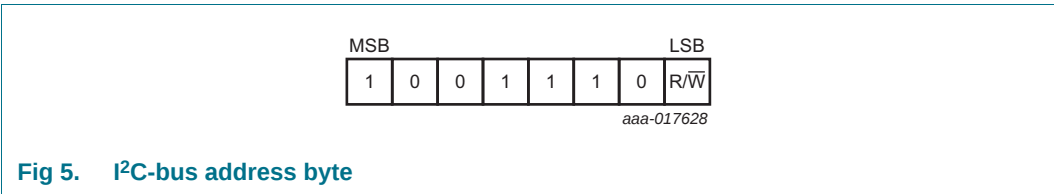
Table 4. Function table

OVERRIDE_N	MUX_SELECT	MUX_OUT OUTPUTS	NON_MUXED_OUT OUTPUT
0	0	All 0s	All 0s
0	1	MUX_IN inputs	Latched NON_MUXED_OUT
1	0	From non-volatile register	From non-volatile register
1	1	MUX_IN inputs	From non-volatile register

[1] Latched NON_MUXED_OUT state will be the value present on the NON_MUXED_OUT output at the time of the MUX_SELECT input transitioned from a logic 0 to a logic 1 state.

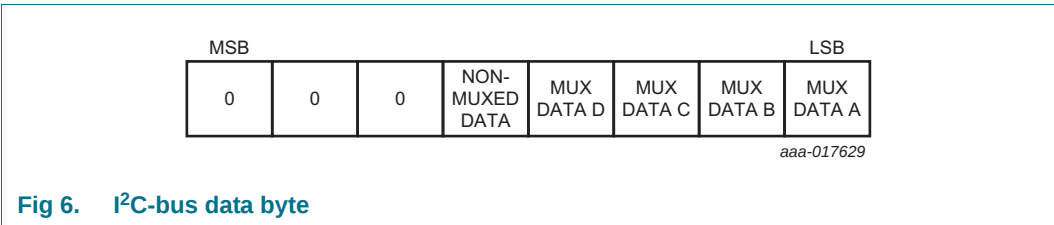
6.2 I²C-bus interface

Communicating with this device is initiated by sending a valid address on the I²C-bus. The address format (see Figure 2) is a fixed unique 7-bit value followed by a 1-bit read/write value which determines the direction of the data transfer.



Following the address and acknowledge bit are 8 data bits which, depending on the read/write bit in the address, will read data from or write data to the non-volatile register. Data will be written to the register if the read/write bit is logic 0 and the WP input is logic 0. Data will be read from the register if the bit is logic 1. The three high-order bits (see Figure 6) are logic 0. The next bit is data which is non-multiplexed. The low four bits are the data which will be multiplexed. A write with any of the first three bits non-zero will be aborted.

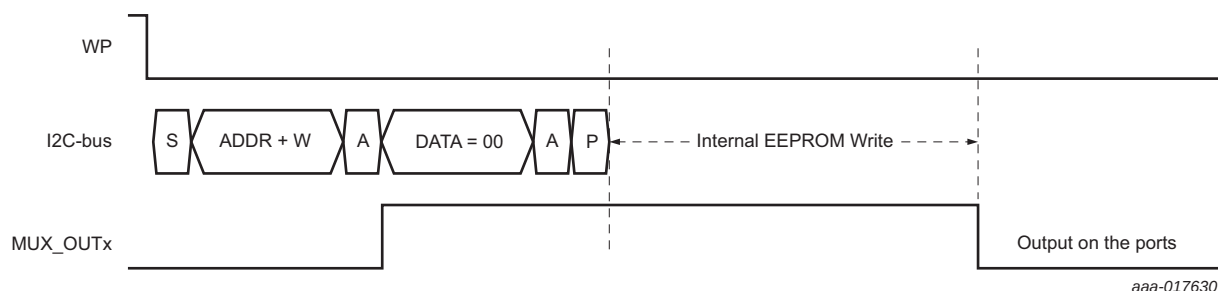
1. To ensure data integrity, the non-volatile register must be internally write protected when V_{CC} to the I²C-bus is powered down or V_{CC} to the component is dropped below normal operating levels.



2. MUX_OUTx will be disabled when the master writes to PCA8550.

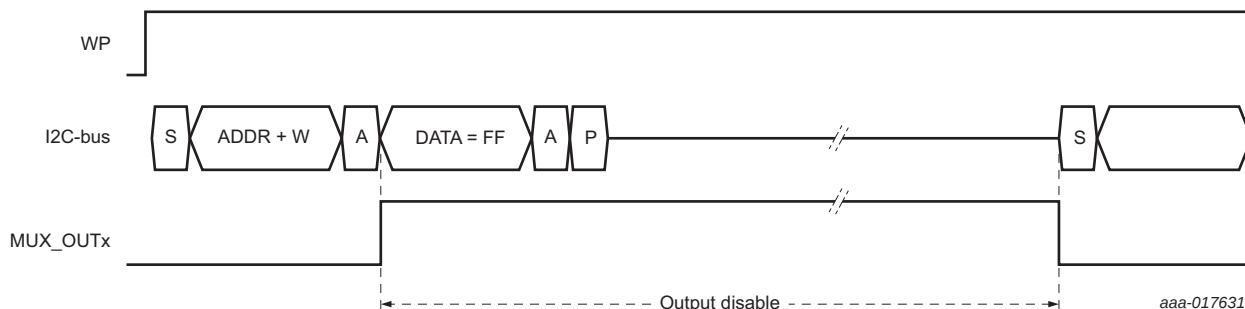
a. With WP enabled, during I²C write cycle the MUX_OUTx will be disabled after the address acknowledge bit and the outputs will be enabled after the internal EEPROM write is completed (Figure 7).

b. With WP disabled, during I²C write cycle the MUX_OUTx will be disabled after the address acknowledge bit and enabled when there is a START condition on the I²C-bus (Figure 8).



MUX_OUTx output after EEPROM write cycle

Fig 7. Write when WP enabled



Do not write to EEPROM when PW is HIGH, the MUX_OUTx will be disabled until another START condition on the I²C-bus

Fig 8. Write when WP disabled

6.3 Power-on reset

When power is applied to VCC, an internal power-on reset holds the PCA8550 in a reset state until VCC has reached VPOR. At that point, the reset condition is released and the PCA8550 volatile registers and I²C state machine will initialize to their default states.

The MUX_OUT and NON_MUXED_OUT pin values depend on:

- the OVERRIDE_N and MUX_SELECT logic levels
- the previously stored values in the EEPROM register/current MUX_IN pin values as shown in [Table 4](#).

7. Limiting values

Table 5. Limiting values [1] [2]

*In accordance with the Absolute Maximum Rating System (IEC 60134).
Voltages are referenced to GND (ground = 0 V).*

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+4.6	V
V _I	input voltage		[3] -1.5	V _{CC} + 1.5	V
V _O	output voltage		[3] -0.5	V _{CC} + 0.5	V
T _{stg}	storage temperature		-60	+150	°C

- [1] Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- [2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.
- [3] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

8. Recommended operating conditions

Table 6. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	DC supply voltage		3.0	3.6	V
V _{POR}	power-on reset voltage	no load; V _I = V _{DD} or V _{SS}	-	2.6	V
V _{IL}	LOW-level input voltage	SCL, SDA; I _{OL} = 3 mA	-0.5	+0.9	V
V _{IH}	HIGH-level input voltage	SCL, SDA; I _{OL} = 3 mA	2.7	4.0	V
V _{OL}	LOW-level output voltage	SCL, SDA; I _{OL} = 3 mA	-	0.4	V
V _{IL}	LOW-level input voltage	OVERRIDE_N, MUX_IN, MUX_SELECT	-0.5	+0.8	V
V _{IH}	HIGH-level input voltage	OVERRIDE_N, MUX_IN, MUX_SELECT	2.0	4.0	V
I _{OL}	LOW-level output current	MUX_OUT NON_MUXED_OUT	-	2.0	mA
I _{OH}	HIGH-level output current	MUX_OUT NON_MUXED_OUT	-	-2.0	mA
Δt/ΔV	input transition rise and fall rate		0	10	ns/V
T _{amb}	ambient temperature	operating in free air	0	+70	°C

9. Static characteristics

Table 7. Static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Input SCL; input/output SDA						
V _{OL}	LOW-level output voltage		0	-	+0.6	V
I _{OL}	LOW-level output current	V _{OL} = 0.4 V	-	-	3	mA
		V _{OL} = 0.6 V	-	-	6	mA
I _{IL}	LOW-level input current	V _{IL} = 0.4 V	−7	-	−32	μA
I _{IH}	HIGH-level input current	V _{IH} = 2.4 V	−1.5	-	−12	μA
V _{hys}	hysteresis voltage		0.19	-	-	V
OVERRIDE_N, WP, MUX_SELECT						
I _{IL}	LOW-level input current		[1] −86	-	−267	μA
I _{IH}	HIGH-level input current		−20	-	−100	μA
MUX_IN_A, MUX_IN_B, MUX_IN_C, MUX_IN_D						
I _{IL}	LOW-level input current	V _{IL} = 0.4 V	−0.72	-	−2.0	mA
I _{IH}	HIGH-level input current	V _{IH} = 2.4 V	−0.72	-	−2.0	mA
MUX_OUT						
V _{OL}	LOW-level output voltage	I _{OL} = 100 μA	−0.3	-	+0.4	V
		I _{OL} = 2.0 mA	−0.3	-	+0.7	V
V _{OH}	HIGH-level output voltage	I _{OH} = −100 μA	2.0	-	2.625	V
		I _{OH} = −1.0 mA	1.7	-	2.625	V
NON_MUXED_OUT						
V _{OL}	LOW-level output voltage	I _{OL} = 100 μA	−0.5	-	+0.4	V
		I _{OL} = 2.0 mA	−0.5	-	+0.7	V
V _{OH}	HIGH-level output voltage	I _{OH} = −100 μA	2.4	-	3.6	V
		I _{OH} = −2.0 mA	2.0	-	3.6	V
I _{CC}	quiescent supply current	V _{CC} = 3.3 V; V _I = 0 V to V _{CC}	-	-	10	mA
		V _I = V _{CC}	-	-	500	μA
C _I	input capacitance		-	-	10	pF
	ESD protection		[2] 2.0			KV
	Input diode clamp voltage		−1.5	-	-	V

[1] V_{hys} is the hysteresis of Schmitt-Trigger inputs

[2] Human body model

10. Dynamic characteristics

Table 8. Dynamic characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t _{MPD}	Mux input to output propagation delay		-	-	20	ns
t _{SOV}	MUX_SELECT to output valid		-	-	22	ns
t _{OVN}	OVERRIDE_N to NON_MUX output delay		-	-	15	ns
t _{OVN}	OVERRIDE_N to mux output delay		-	-	25	ns
t _r	rise time	output	1.0	-	3	ns/V
t _f	fall time	output	1.0	-	3	ns/V
C _L	load capacitance	test load on outputs	-	-	15	pF

Table 9. I²C-bus dynamic characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f _{SCL}	SCL clock frequency		10	400	kHz
t _{HIGH}	HIGH period of the SCL clock		600	-	ns
t _{LOW}	LOW period of the SCL clock		1.3	-	ns
t _{SP}	pulse width of spikes that must be suppressed by the input filter		0	50	ns
t _{SU,DAT}	data set-up time		100	-	ns
t _{HD,DAT}	data hold time		0	-	ns
t _r	rise time of both SDA and SCL signals	10 pF to 400 pF bus	20	300	ns
t _f	fall time of both SDA and SCL signals	10 pF to 400 pF bus	20	300	ns
t _{BUF}	bus free time between a STOP and START condition		1.3	-	ns
t _{SU,STA}	set-up time for a repeated START condition		600	-	ns
t _{HD,STA}	hold time (repeated) START condition		600	-	ns
t _{SU,STO}	set-up time for STOP condition		600	-	ns
C _b	capacitive load for each bus line		-	400	pF
T _{cy(W)}	write cycle time ^[1]		TYPICAL = 15		ms

[1] WRITE CYCLE time can only be measured indirectly during write cycle. The device will not acknowledge its I²C address.

11. Non-volatile storage specifications

Table 10. Non-volatile storage specifications

Parameter	Specification
memory cell data retention	10 years (minimum)
number of memory cell write cycles	100,000 cycles (minimum)

Application note AN250, "I²C DIP Switch" provides additional information on memory cell data retention and the minimum number of write cycles.

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

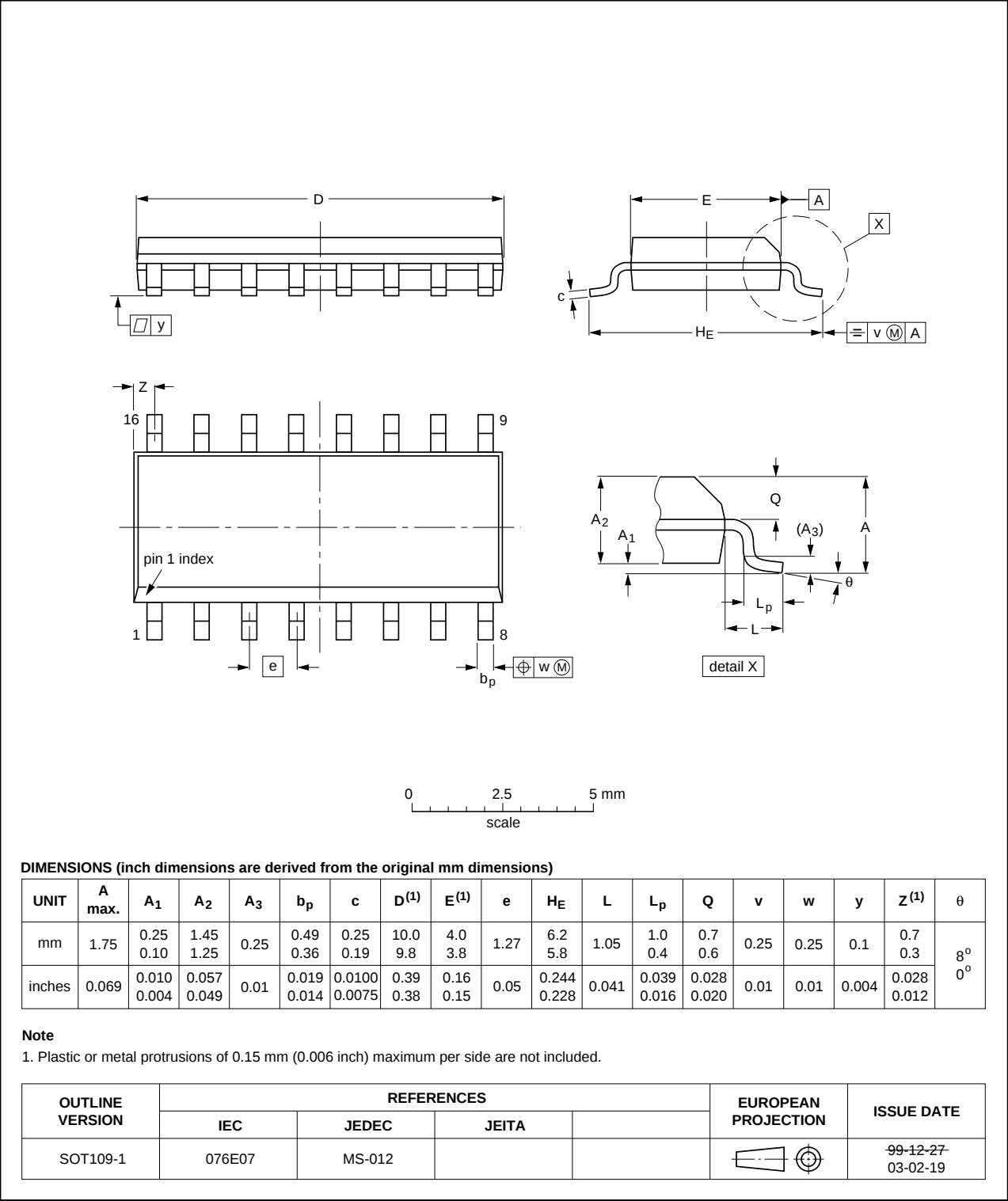


Fig 9. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

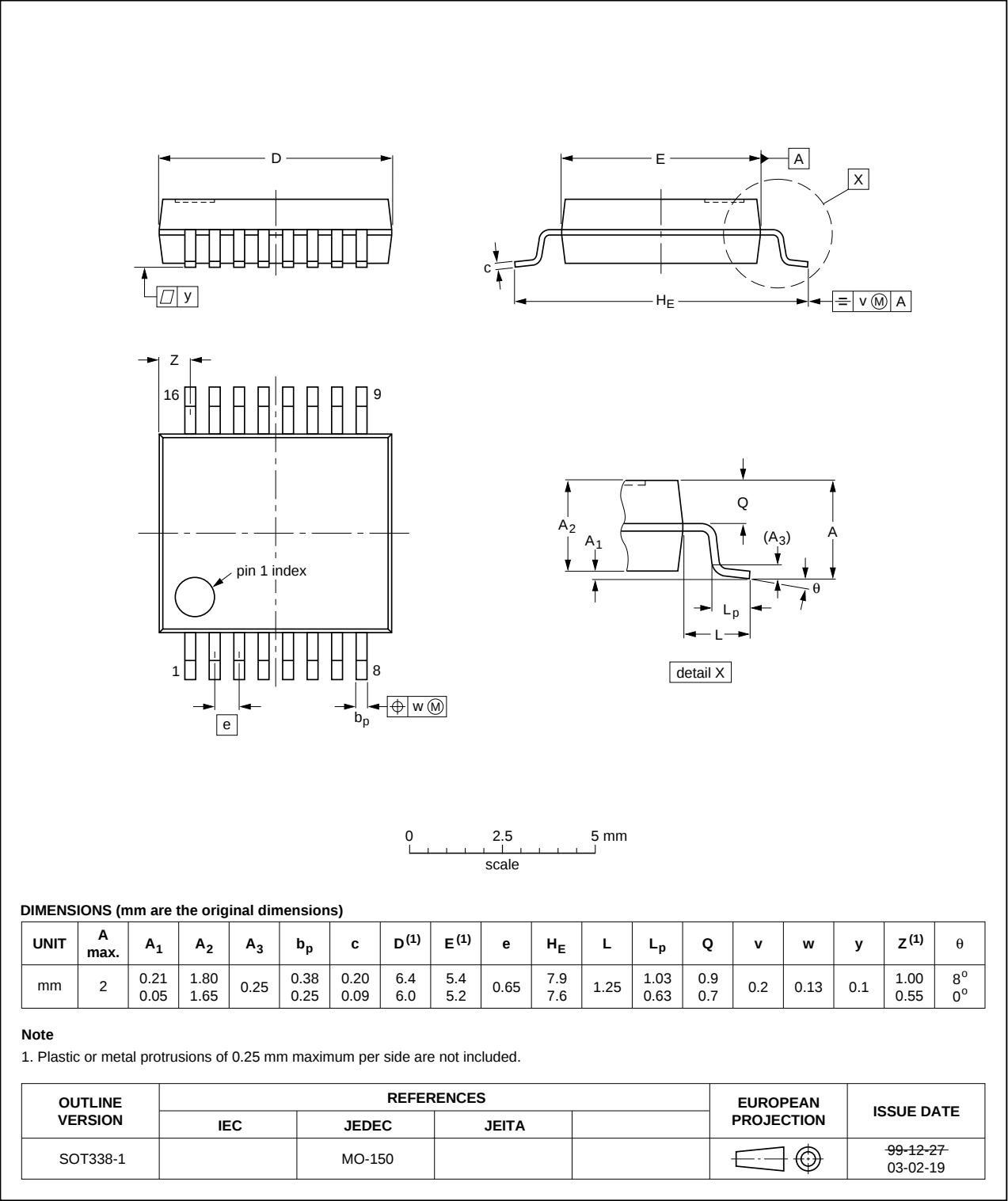


Fig 10. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

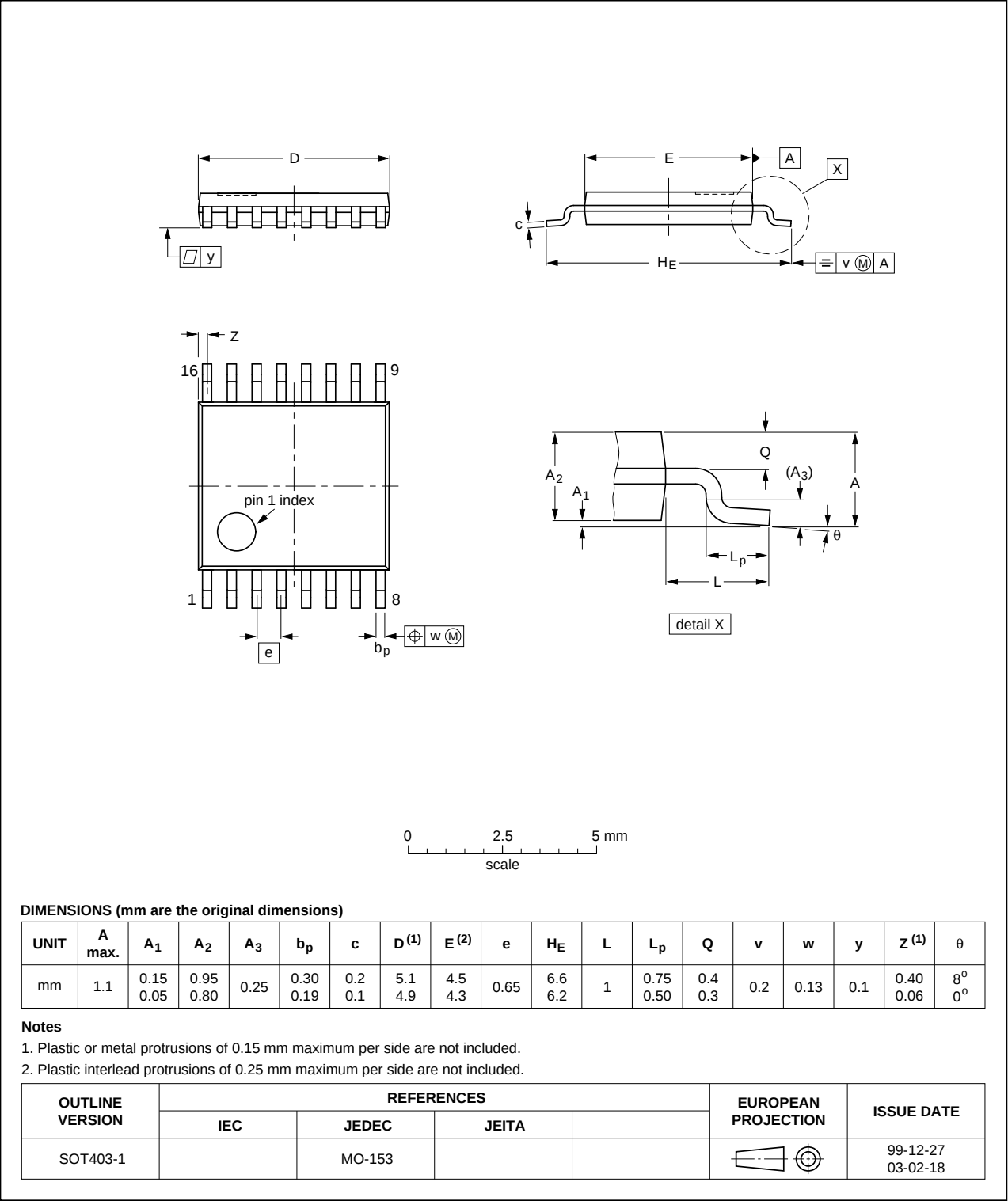


Fig 11. Package outline SOT403-1 (TSSOP16)

13. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note AN10365 “Surface mount reflow soldering description”.

13.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

13.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leadless or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leadless SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leadless packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

13.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

13.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 12](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 11](#) and [12](#)

Table 11. SnPb eutectic process (from J-STD-020D)

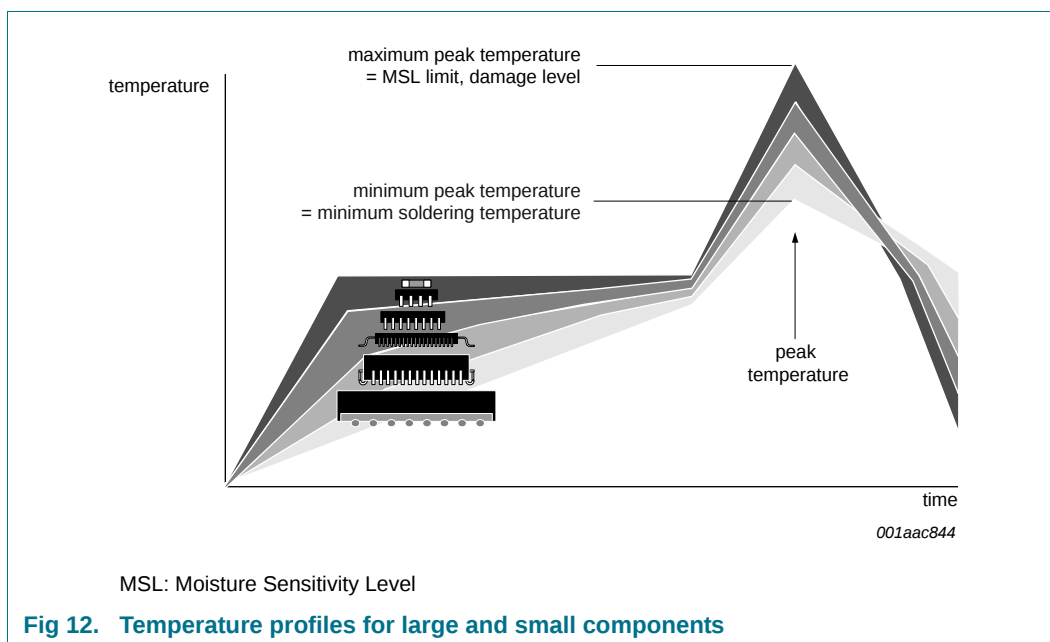
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm ³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 12. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm ³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 12](#).



For further information on temperature profiles, refer to Application Note AN10365 "Surface mount reflow soldering description".

14. Soldering: PCB footprints

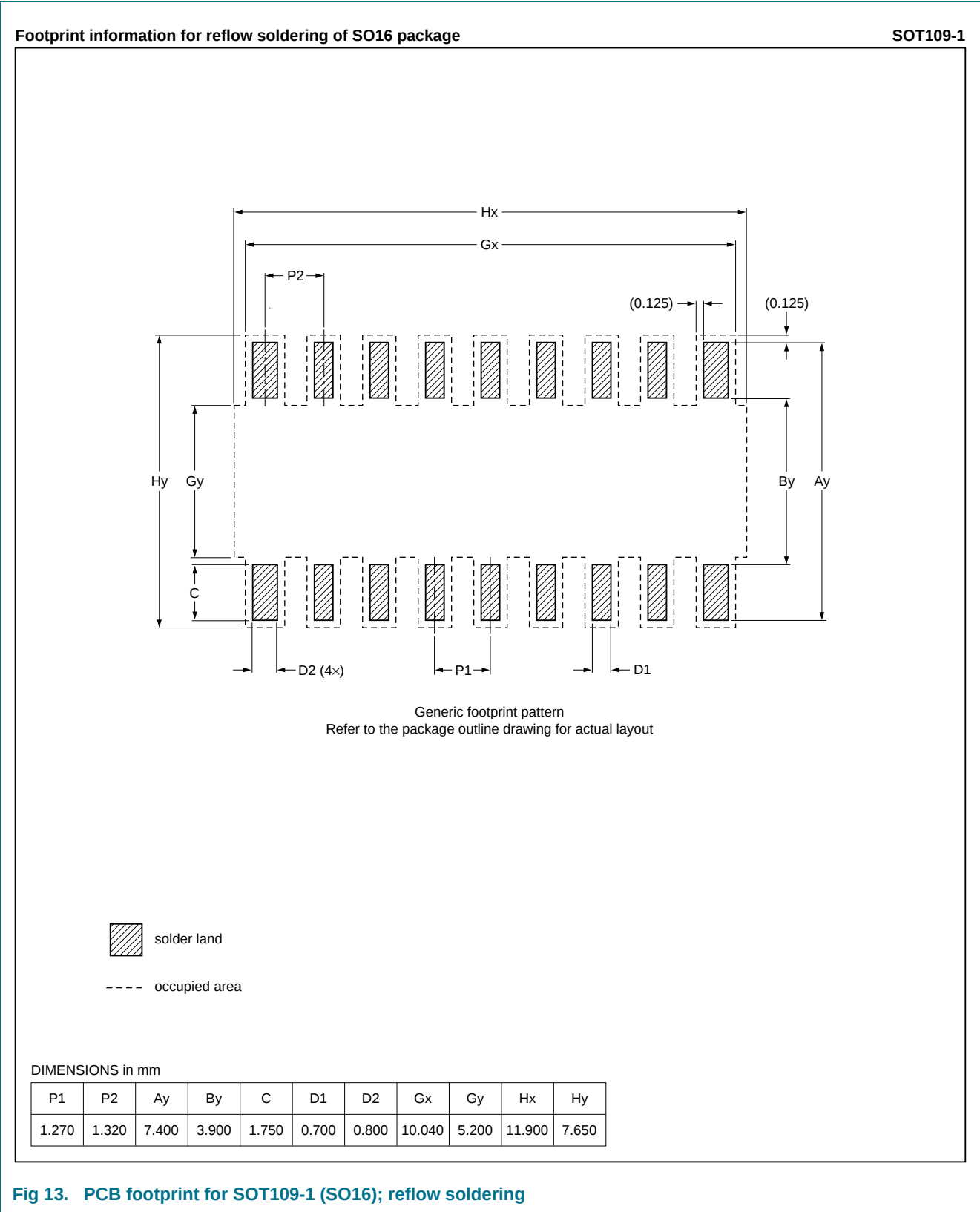


Fig 13. PCB footprint for SOT109-1 (SO16); reflow soldering

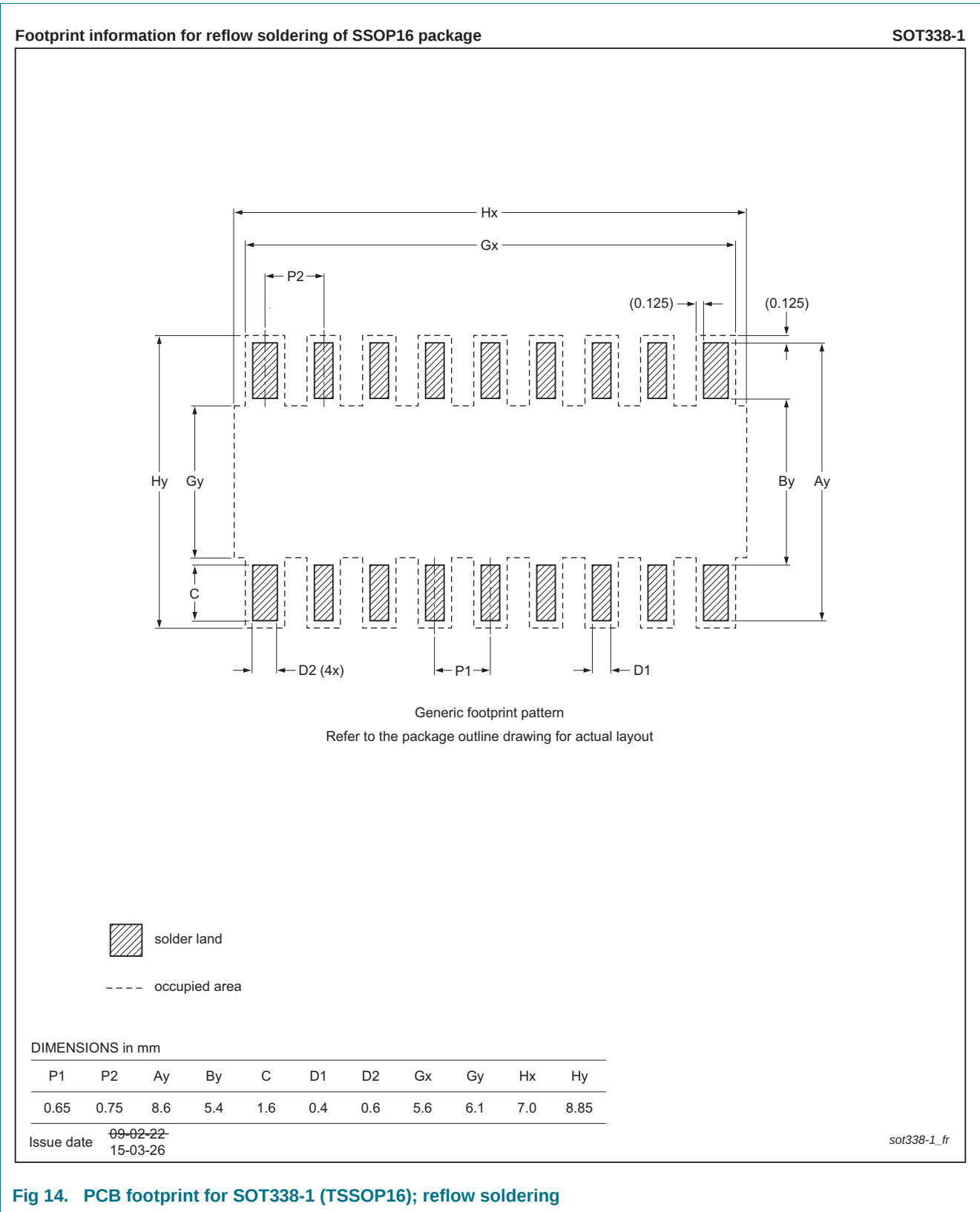
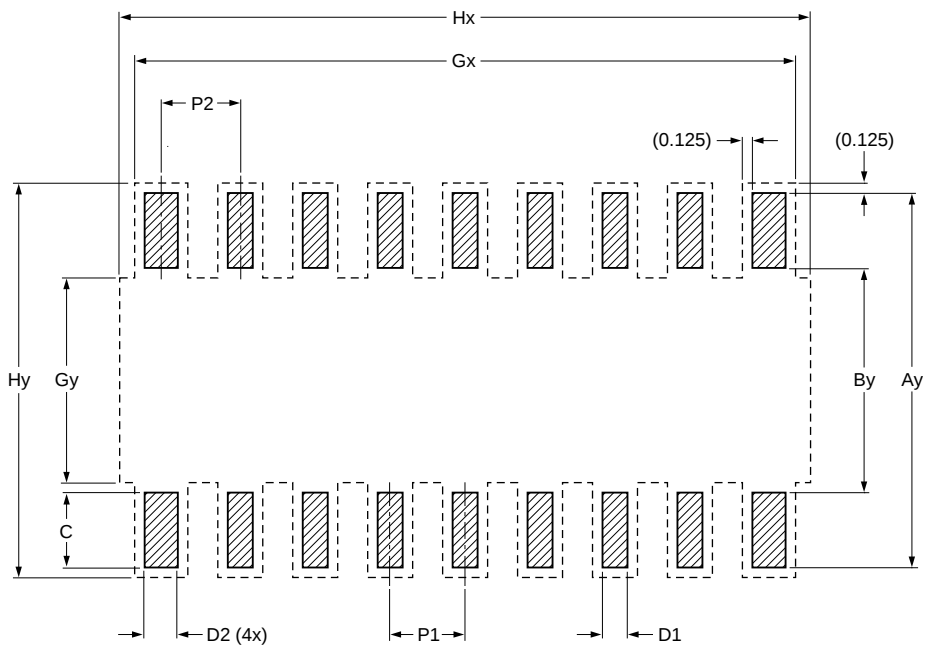


Fig 14. PCB footprint for SOT338-1 (TSSOP16); reflow soldering

Footprint information for reflow soldering of TSSOP16 package
SOT403-1



Generic footprint pattern
Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ay	By	C	D1	D2	Gx	Gy	Hx	Hy
0.650	0.750	7.200	4.500	1.350	0.400	0.600	5.600	5.300	5.800	7.450

sot403-1_fr

Fig 15. PCB footprint for SOT403-1 (TSSOP16); reflow soldering

15. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA8550 v.7	20150408	Product data sheet	-	PCA8550 v.6
Modifications:	- The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. - Legal texts have been adapted to the new company name where appropriate. - Updated Section 6.2.			
PCA8550 v.6	20030627	Product data sheet	-	PCA8550 v.5
PCA8550 v.5	20010112	Product data sheet	-	PCA8550 v.4

16. Legal information

16.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

16.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

16.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the

product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

16.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

17. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

18. Contents

1	General description	1
2	Features and benefits	1
3	Ordering information	2
3.1	Ordering options	2
4	Block diagram	3
5	Pinning information	4
5.1	Pin description	4
6	Functional description	5
6.1	Function table	6
6.2	I ² C-bus interface	6
6.3	Power-on reset	7
7	Limiting values	8
8	Recommended operating conditions	8
9	Static characteristics	9
10	Dynamic characteristics	10
11	Non-volatile storage specifications	10
12	Package outline	11
13	Soldering of SMD packages	14
13.1	Introduction to soldering	14
13.2	Wave and reflow soldering	14
13.3	Wave soldering	14
13.4	Reflow soldering	15
14	Soldering: PCB footprints	17
15	Revision history	20
16	Legal information	21
16.1	Data sheet status	21
16.2	Definitions	21
16.3	Disclaimers	21
16.4	Trademarks	22
17	Contact information	22
18	Contents	23

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP Semiconductors N.V. 2015.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 8 April 2015

Document identifier: PCA8550